Submitted By: U19CS012 (D-12)

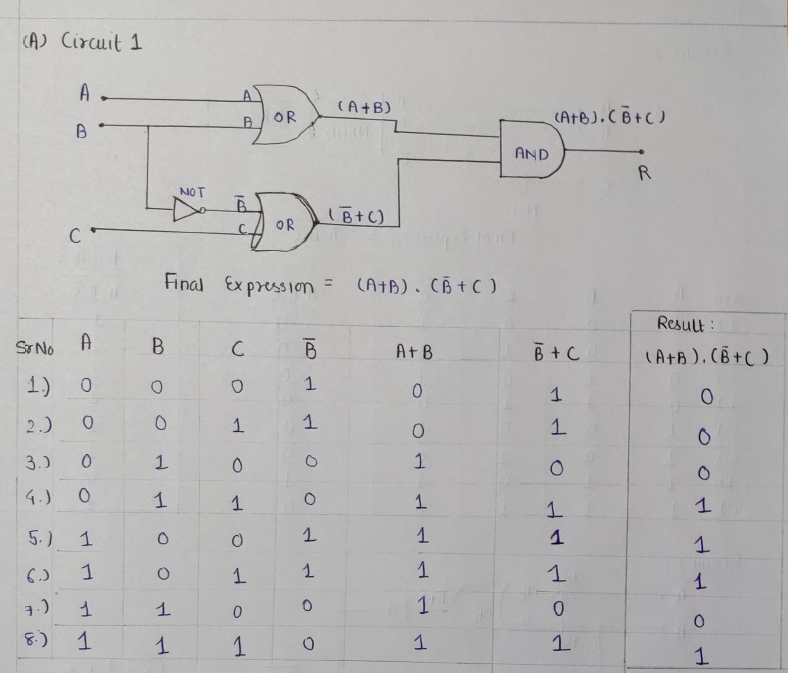
BHagya vinod rANA | c.s.e., S.V.N.I.T.

DIGITAL ELECTRONICS & LOGIC DESIGN LAB

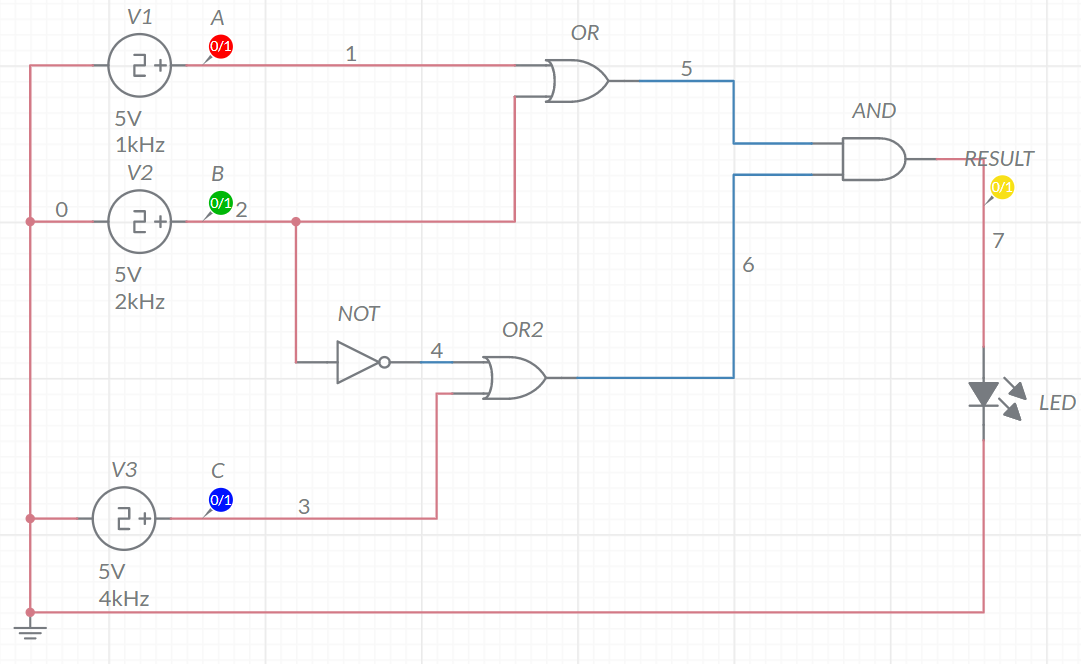
LAB 2 (20 AUG): Assignment – LOGIC CIRCUIT

**Question –1**

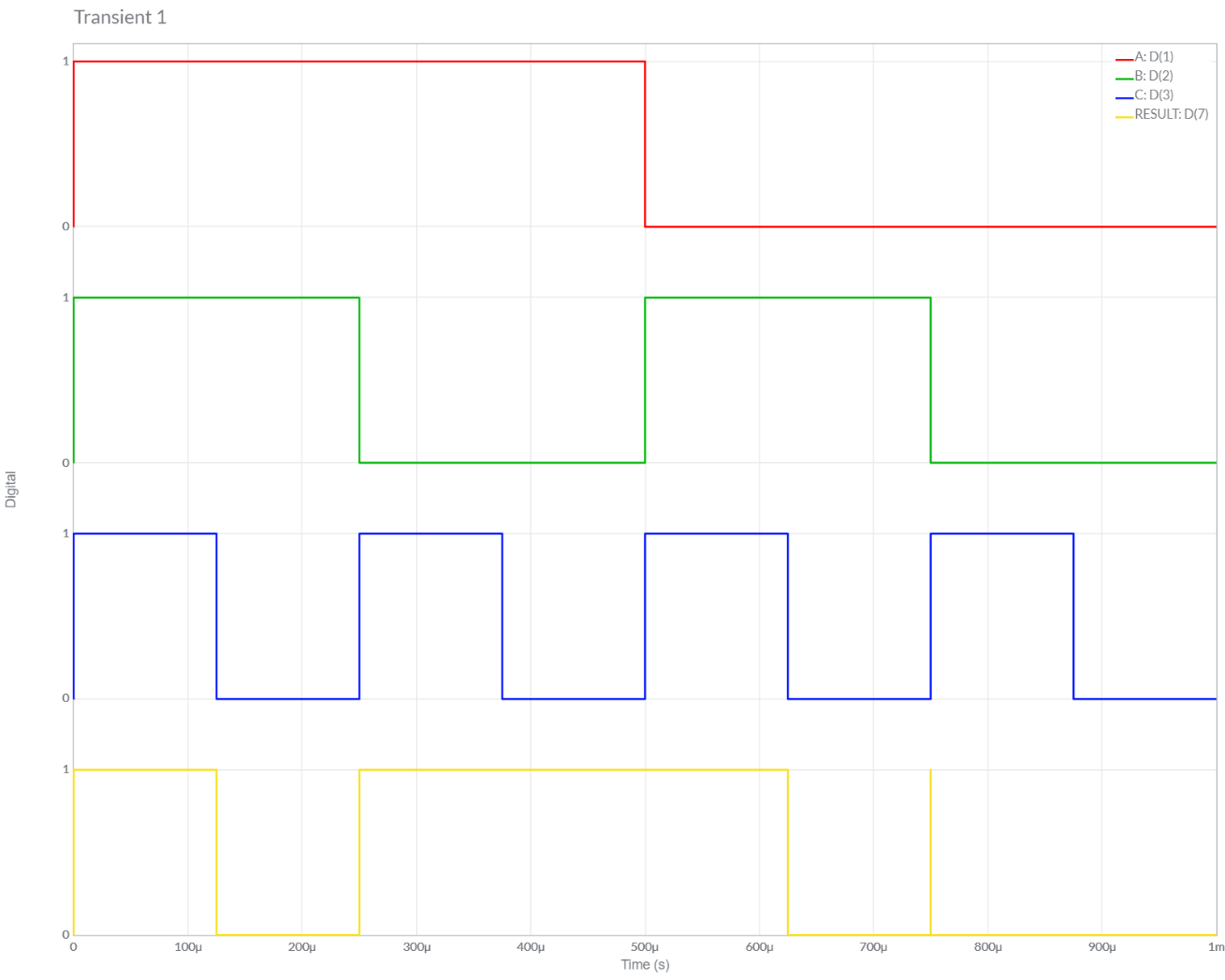
*a.) Calculate the Logic Gates Circuit’s Output [Theoretical]*



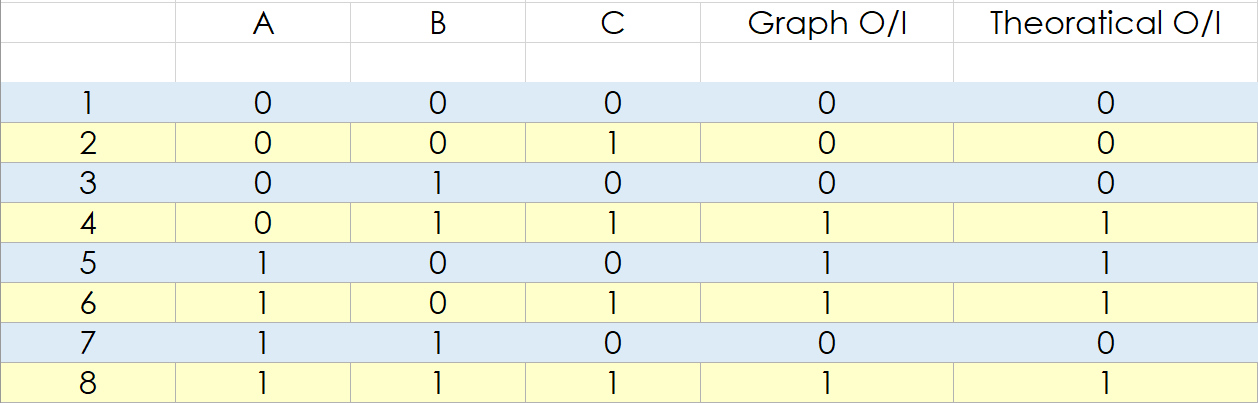
*b.) Implement the circuit as shown in Figure in Multisim online.*



*c.) Time Graph*

**

*d.) Final Result and Conclusion*



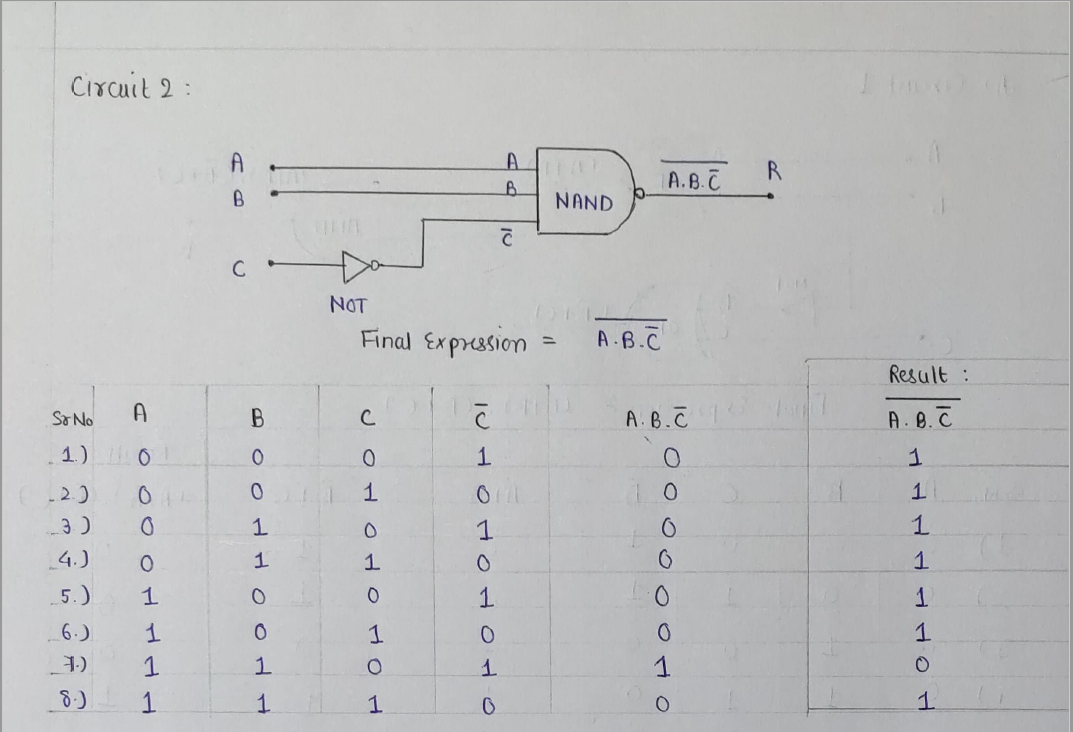
*Conclusion:*

We can observe from Above Table, Both the *Theoretical* and *Multisim* Values of Given Circuit are **Equal**.

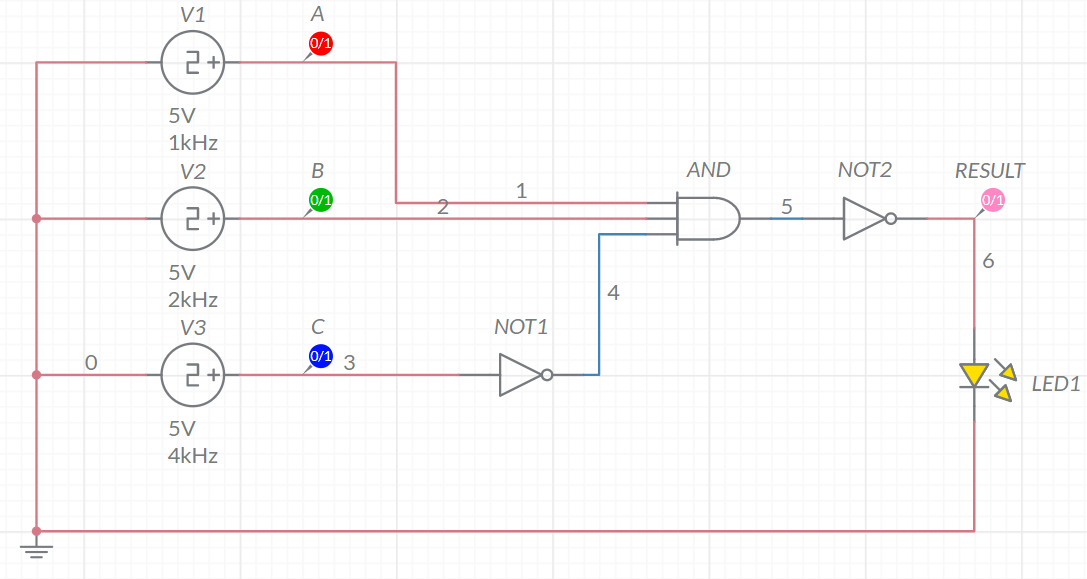
Hence, Experiment is Performed Successfully (without any Error).

**Question –2**

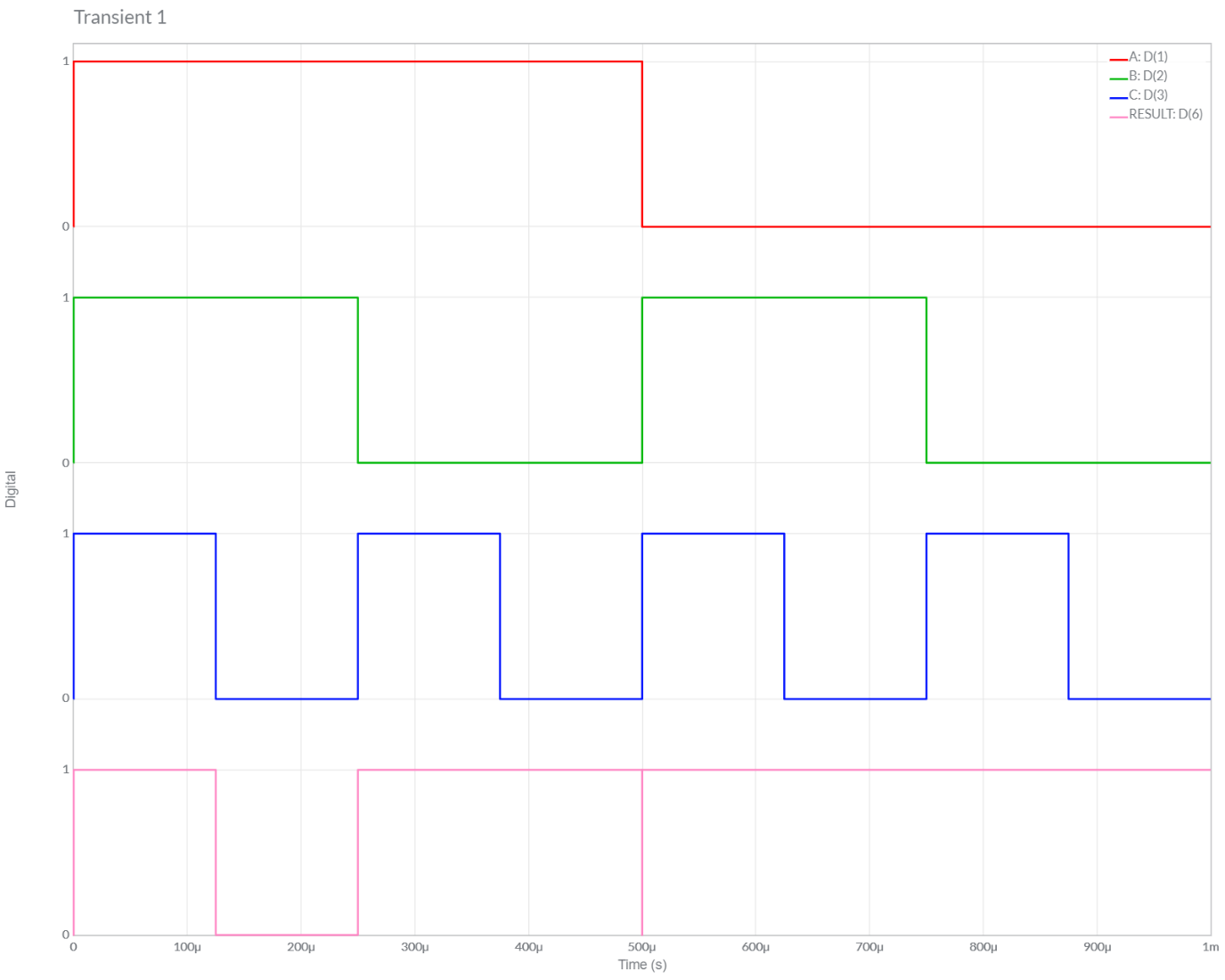
*a.) Calculate the Logic Gates Circuit’s Output [Theoretical]*



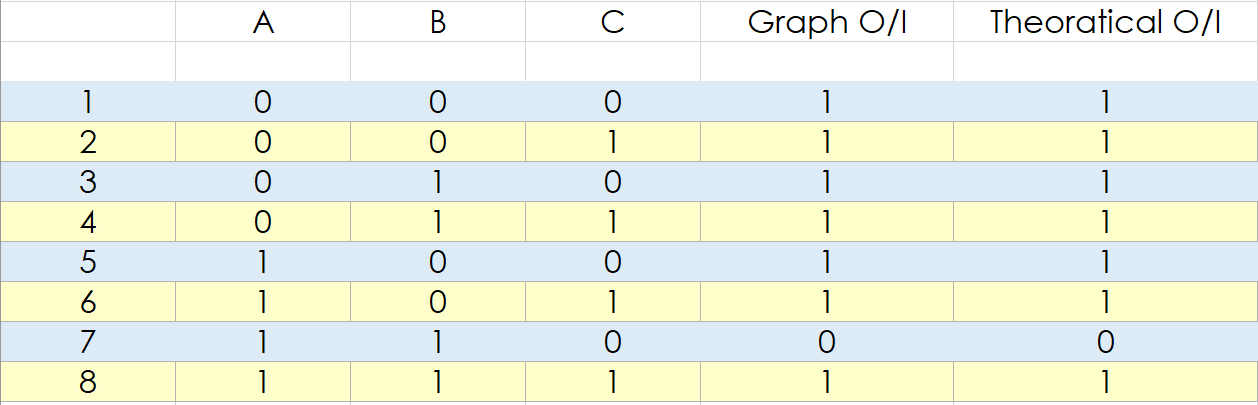
*b.) Implement the circuit as shown in Figure in Multisim online.*



*c.) Time Graph*

**

*d.) Final Result and Conclusion*



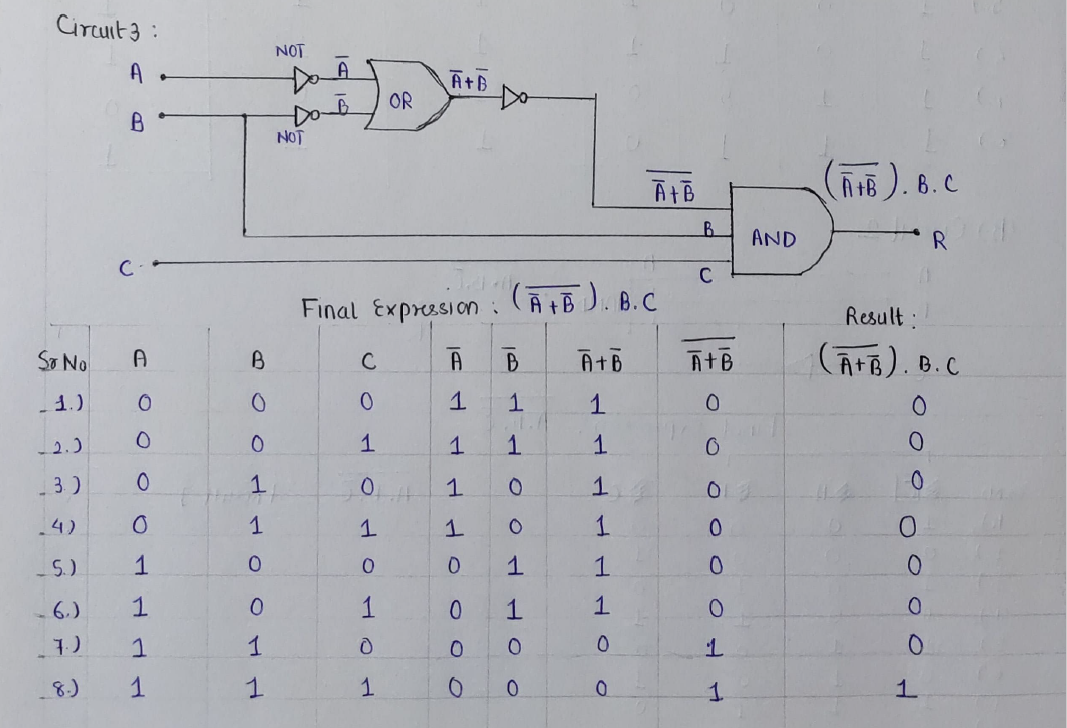
*Conclusion:*

We can observe from Above Graph, Both the *Theoretical* and *Multisim* Values of Given Circuit are **Equal**.

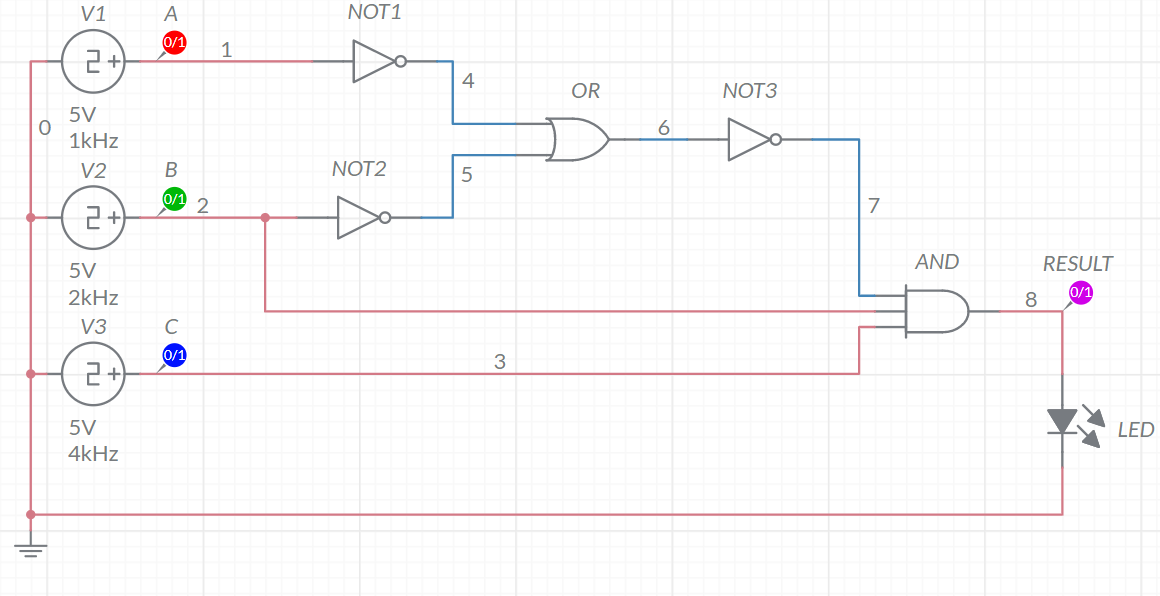
Hence, Experiment is Performed Successfully (without any Error).

**Question –3**

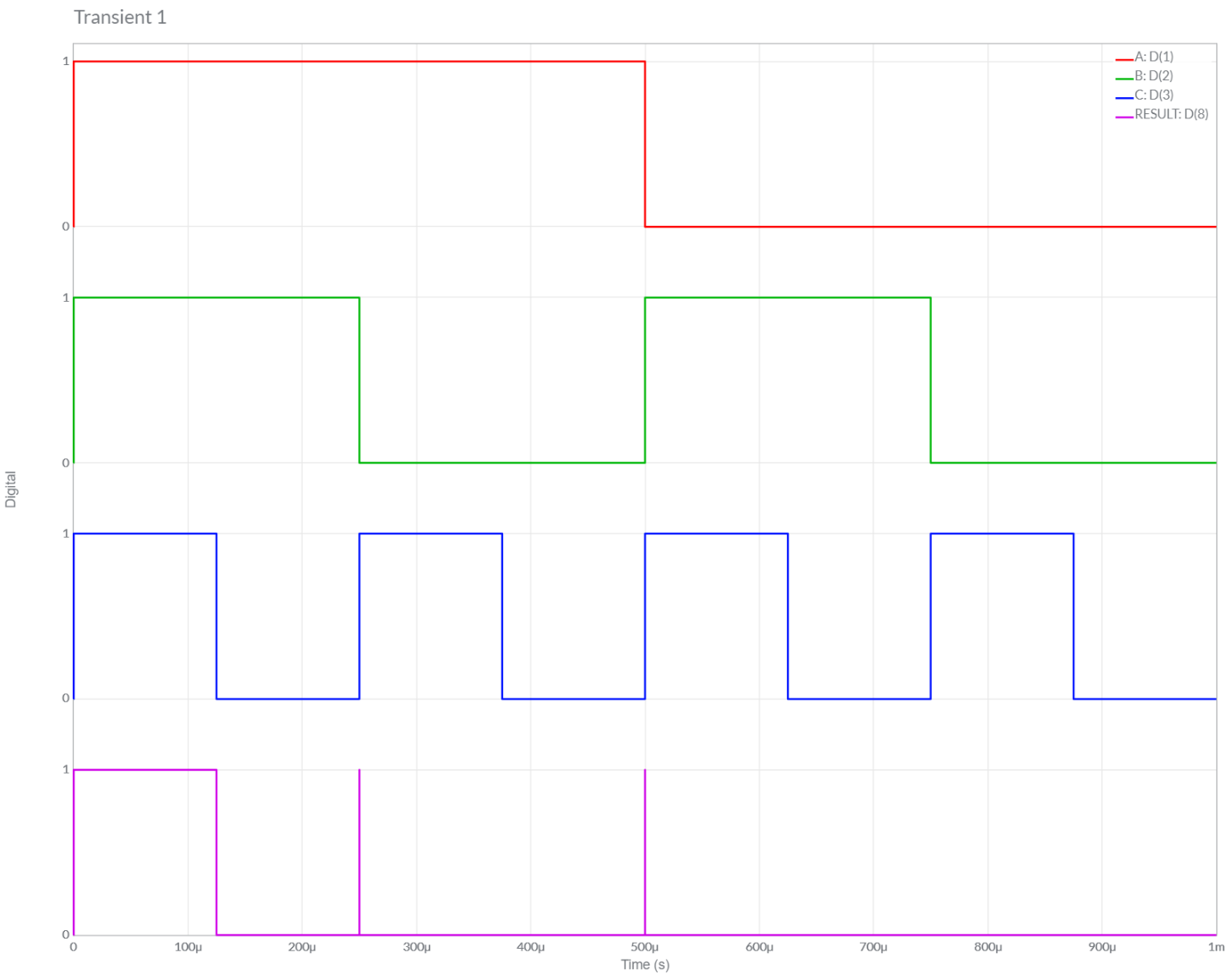
*a.) Calculate the Logic Gates Circuit’s Output [Theoretical]*



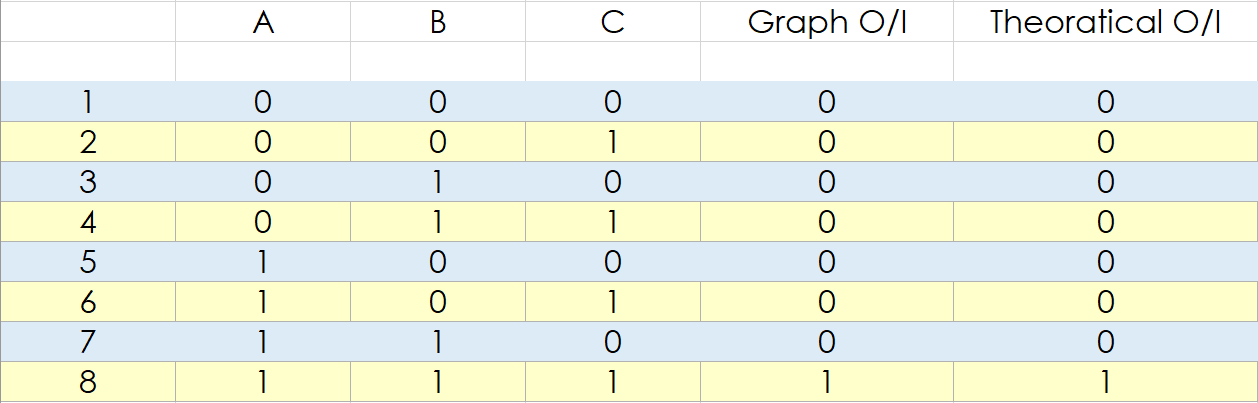
*b.) Implement the circuit as shown in Figure in Multisim online.*



*c.) Time Graph*

**

*d.) Final Result and Conclusion*



*Conclusion:*

We can observe from Above Table, Both the *Theoretical* and *Multisim* Values of Given Circuit are **Equal**.

Hence, Experiment is Performed Successfully (without any Error).

Submitted By:

Roll Number: U19CS012 (D-12)

Name: Bhagya Rana